Methodology for Analyzing ESD-Induced Soft Failure Using Full-Wave Simulation and Measurement

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***Abstract*—An analysis methodology is presented to investigate soft failures in electronic devices. This methodology combines transmission line pulse (TLP) full-wave simulations with system-level and TLP measurements. Information on susceptible parts in the device under test (DUT) and/or soft failure sensitivity of the integrated circuits (ICs) are obtained from the measurements. Then, the TLP current spreading within the printed circuit board (PCB) of the DUT is simulated. The susceptible signals can be determined by comparing the simulated voltages and/or currents at the signal terminations with the measured threshold values. If the simulated voltages and/or currents are higher than the threshold values, the signal is considered susceptible and a soft failure may occur in the DUT. Using the obtained information from simulations and measurements, the root causes of soft failures can be identified. Further, by utilizing full-wave simulations, the design of the product can be modified to reduce the electrostatic discharge (ESD) noise on the susceptible signals, and consequently prevent soft failures. The proposed analysis methodology is applied to a tablet which suffers from soft failure. The root cause of the soft failure is identified, and countermeasures are designed against the ESD-induced soft failure.**

***Index Terms*—Electromagnetic analysis, electromagnetic interference, electronic device, electrostatic discharge (ESD), soft failure.**

I. Introduction

ELECTROSTATIC discharge to an electronic device may lead to two different kinds of failures, referred to as hard and soft failures [1]. A small amount of energy delivered to the device can cause a soft failure. Unlike hard failures, ESD-induced soft failures do not cause any damage to the device and they do not leave any physical trace. Therefore, it is difficult to identify the ESD noise coupling path. Momentary unexpected responses corrected automatically, unexpected responses requiring user intervention, a change in the operating state, device reset, and device power off or on are the general categories of soft failures [2]. These failures can be caused by signal integrity violations, by out of band voltages reaching the ESD protection level clipping values, and may trigger logical errors inside the IC far away from the I/O which coupled the noise current into the IC.

Recently, ESD-induced soft failures have been investigated in different aspects. In [3] and [4], the effect of system activity on ESD-induced soft failures was studied. Performing some ESD measurements on single-board computers, it was shown in [3] that the occurrence of a specific soft failure depends on the program running on the system at the time of the failure. A more systematic investigation on the relationship between the ESD-induced soft failure and the running application on the system was performed in [4]. In that work, the ESD susceptibility of the central processing unit (CPU) IC of a cell phone was related to the near field of the IC by obtaining the correlation between the TLP and electromagnetic interference maps of the IC. In [5], soft failures were induced to a circuit board containing a custom test chip and the root causes of the failures were ascertained. It was shown that while ESD noise is similar for tethered and mobile DUTs, more charge is injected into a tethered DUT which makes it more susceptible to ESD.

There are some experimental methods to predict ESD-induced soft failures on electronic devices [6]. These methods can be applied to devices that do not have finalized hardware and software making modifying the design of the device less costly. However, since the root cause of the soft failure cannot be determined by these methods, they cannot offer approaches to improve the design of the product. Therefore, developing methods to analyze ESD-induced soft failures and identify the root causes of these failures is of interest.

In [7], an 18 MHz D flip–flop IC was characterized by obtaining its behavioral model. The failure triggering of the IC was predicted by combining the developed behavioral model of

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the IC with a full-wave model consisting of the ESD generator. In [8], the soft failure occurrence was investigated by modeling a microcontroller (Arduino Uno) by an *RC* circuit. In [9], hard and soft failures caused by system-level ESD stress on the liquid crystal display (LCD) module of a mobile phone were investigated, which showed the soft and hard failures occurred with similar discharge mechanisms. A systematic methodology was presented in [10] and [11] to analyze ESD-induced soft failure in mobile phones. The proposed method was based on ESD simulation and ESD characterization of the device. The mobile phone, ESD generator, and horizontal coupling plane (HCP) setup were modeled in full-wave simulation to find ESD current paths on the phone, as well as the signals with high voltages and currents. Then, by performing an ESD test on the ESD-sensitive signals, the signals which caused the soft failures were detected.

Here, the method presented in [10] is expanded to analyze soft failures in electronic devices. Similar to [10], the proposed method requires the device to be tested according to IEC61000-4-2 [12]. Both methods can guide system improvements by providing in-depth understanding of the root cause of the soft failure. Although both methods are similar in this regard, they have some differences as follows.

1) In [10], air discharge was used for system-level testing [12]. Since the air discharge current cannot be simulated without including arc resistance laws and knowledge of the arc length [13], the excitation current in full-wave simulation is obtained from measuring the air discharge current to the DUT. In the proposed method, measured TLP injected current is used as the excitation current in the full-wave simulation. The TLP injected current is better controlled and more suitable for a clean injection with less noise coupling to the oscilloscope.
2) In [10], direct injection with an ESD generator was performed on the DUT to quantify the sensitivity of only those nets which can be reached. In the proposed method, near-field scanning [14] is performed on the DUT to identify the sensitive regions. The sensitive regions would not be identified without scanning as many traces are not accessible for direct injection. Further, this allows coupling through the package into the IC. Then, TLP direct injections are performed on susceptible regions and traces to quantify the sensitivity of the nets.
3) Since TLP direct injection is used in the proposed method, highly sensitive nets can be tested without disturbing the system. For example, the injection can be done via a 1-pF capacitor to minimize the effect on the signal integrity. However, direct injection with an ESD generator as presented in [10] at a highly sensitive signal will disturb system functionality.
4) Complex root causes of the soft failures such as weak couplings (< -40 dB) between signals can be identified by using the proposed method.
5) In the proposed method, the simulation model is simplified based on ESD and TLP measurements. This decreases the complexity of the numerical model as well as the computational resources. However, the simulation model in [10] was not simplified and all the details of the DUT such as PCBs, transient voltage suppression (TVS) diodes, flex cables, LCD, antenna, and passives were considered in the model. This leads to very large complex models, and the need to add many components such as estimated impedances for the IC pins, passive components, etc. Further, the problem of model verification is significantly more complex in the previously suggested method.

In the proposed method, TLP full-wave simulation on the simplified PCB of the DUT is performed after obtaining the ESD susceptibility of the DUT and soft failure sensitivity of the DUT IC pins by performing ESD and TLP measurements. Since TLP simulation is used in this method, there is no need to consider the ESD generator model [10], [11], [15]–[18] and system mechanical design in the simulation, as is the case for contact mode ESD simulations based on the HCP setup. This significantly reduces computational resources. If the simulated voltages and/or currents at the terminations of the signals are higher than the corresponding soft failure sensitivity data of the DUT obtained from measurements, a soft failure can occur. The root cause of the soft failure can then be identified by the obtained information from simulation and ESD and TLP measurements. Knowing the root cause of the soft failure and utilizing full-wave simulations, the design of the DUT can be modified to reduce the TLP noise on the susceptible signals and prevent soft failures.

The developed methodology to analyze ESD-induced soft failures in electronic devices is presented in Section II. In Section III, this methodology is applied to a tablet which suffers from soft failure when ESD is injected to some specific locations of the tablet ground (GND). Utilizing the proposed methodology, the root cause of the soft failure in the tablet is identified. Also, by using full-wave simulations, the design of the PCB layout is modified in such a way that no failure due to ESD is expected in the modified design. The conclusion is given in Section IV.

II. Methodology

The proposed methodology for analysis of soft failures caused by ESD is shown in the flowchart in Fig. 1. As the first step, the system-level ESD test according to the international ESD testing standard IEC 61000-4-2 [12] is performed on the DUT to identify the following aspects.

1) Positions on the DUT at which injecting ESD causes soft failure.
2) The effect of different conditions of the DUT on the soft failure behavior (examples of these conditions include placing the DUT with display down, DUT with display up, and system on chip (SoC) shielded or not shielded).
3) Soft failure signatures.
4) Threshold voltage of the ESD generator at which soft failure occurs.

The second step is to perform TLP susceptibility scanning to identify susceptible regions and nets. The susceptibility scanning is performed based on the DUT conditions as well as

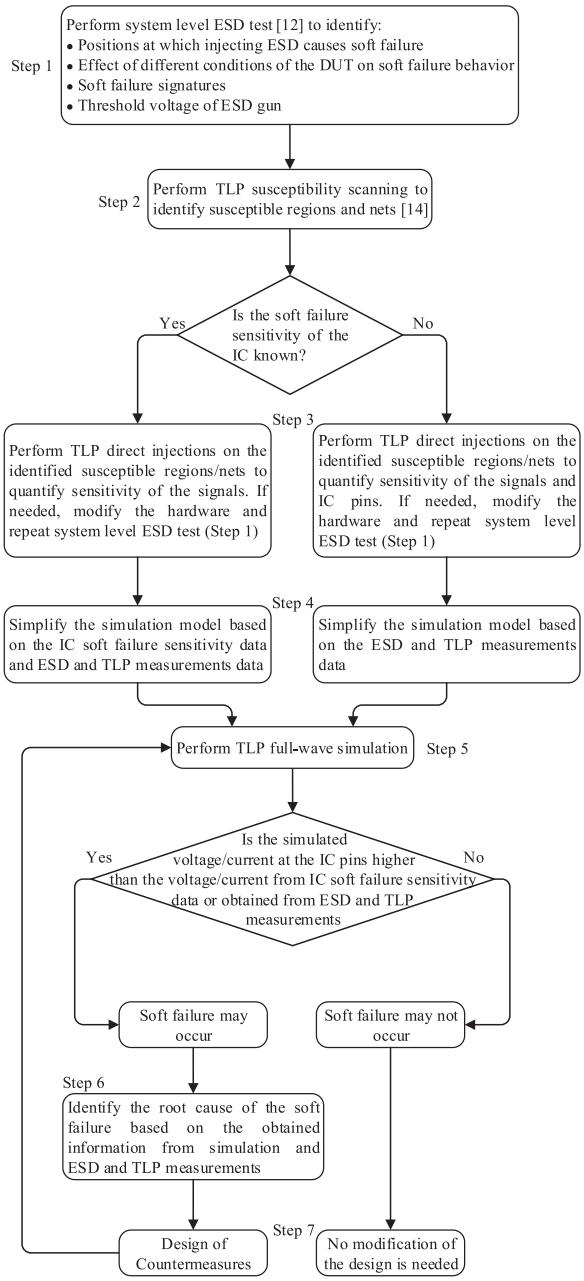


Fig. 1. Flowchart of the proposed methodology for the analysis of ESD-induced soft failure.

injection positions for which soft failure occurred during system-level ESD testing (Step 1). For instance, if a soft failure occurred by injecting ESD at a connector of the DUT in Step 1, then the connector region is scanned in Step 2.

In Step 3, TLP direct injections are performed on the susceptible regions and nets which are identified in Step 2 to quantify sensitivity of the signals and IC pins. Here, high impedance injection methods may be used to avoid disturbing the signal integrity. If the soft failure sensitivity data of the IC are available, there is no need to perform TLP direct injections on the IC pins if those pins are in the identified sensitive regions. If the IC soft failure sensitivity is not available, it is not possible to characterize all pins of the IC since the TLP measurements are performed on the final product where the IC is mounted on the PCB and some of the IC pins may be inaccessible. Regarding the results obtained from TLP direct injections, the hardware of the DUT may be modified for performing the system-level ESD test. In this test, any change in the soft failure occurrence due to the hardware modification is investigated. This investigation can be used later to identify the root cause of the failure.

In Step 4, the simulation model of the PCB of the DUT is simplified based on the ESD and TLP measurements. In this step, only susceptible regions of the PCB are considered in the simulation. Also, only the susceptible signals and IC pins are terminated by passive elements and there is no need to substitute all the active elements by their corresponding passive models. These simplifications significantly decrease the simulation model complexity, computational resources needed, and also reduce the difficulty posed by model verification.

In Step 5, TLP full-wave simulation is performed by using the obtained information from TLP direct injections in Step 3. Based on this information, the voltage/current excitation waveform and the position of the excitation are defined in the simulation. Then, the simulated voltages/currents at the susceptible IC pins are compared with the threshold voltages/currents at the corresponding pins obtained from Step 3 and the IC soft failure sensitivity, if available. If the simulated voltages/currents are higher than the threshold values, then the occurrence of the soft failure may be possible.

In Step 6, the root cause of the soft failure is identified by utilizing the obtained information from full-wave simulations and ESD and TLP measurements. Based on the identified root cause of the soft failure, the design of the PCB of the DUT is modified in Step 7 so that the root cause of the failure is eliminated. Then, by simulating the modified model (Step 5), the occurrence of the soft failure is investigated. The PCB design is then improved until no soft failure is predicted by the proposed methodology.

III. Case Study

The presented methodology was utilized to analyze the ESD-induced soft failure in a tablet. The structure of the tablet is shown in Fig. 2. In this DUT, soft failures occurred when ESD was injected at the shells of the high-definition multimedia interface (HDMI) and secure digital (SD) card, even if these components were not active.

A. System-Level ESD Test (Step 1)

To characterize the soft failures of the DUT, ESD was injected on the shells of the HDMI, universal serial bus (USB), SD card, and subscriber identity module (SIM) card connectors with a Teseq ESD generator. The DUT was placed on an HCP setup according to IEC 61000-4-2 standard [12]. The HCP setup is shown in Fig. 3. An insulation sheet with 0.5 mm thickness and 2.6 dielectric constant was placed between the DUT and HCP. The ESD was injected with direct contact to the ground of the HDMI and USB cables. To discharge ESD on the SD and SIM cards, a piece of copper tape was soldered to the SD and SIM card shells and the contact discharge was performed on

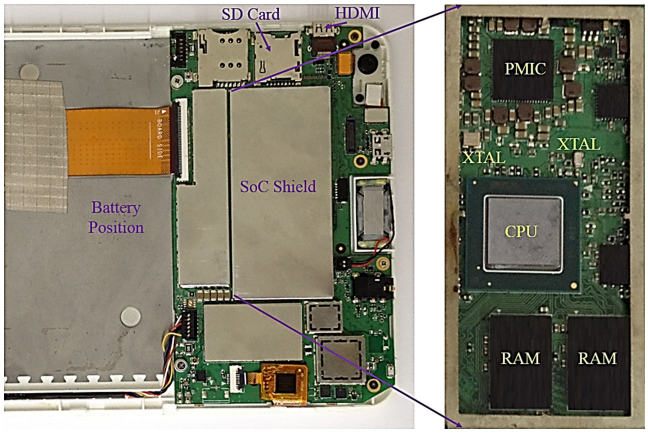


Fig. 2. Structure of the tablet.

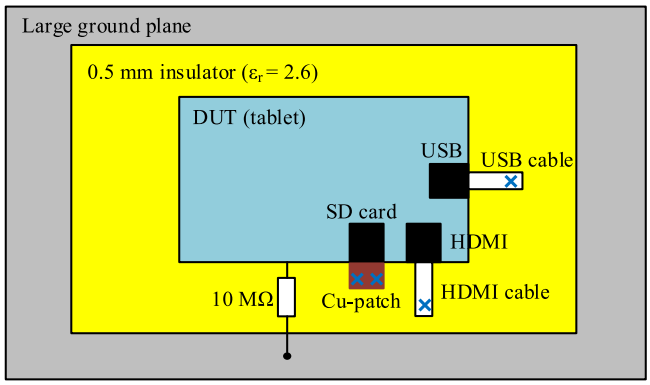


Fig. 3. Measurement setup for system-level ESD test (crosses show the positions of ESD injections).

TABLE I
SUMMARY OF SYSTEM-LEVEL ESD TEST (STEP 1)

Zap position	SoC shield	Threshold voltage
HDMI cable GND	No	5 kV
HDMI cable GND	Yes	5 kV
Cu-tape soldered to SD card	No	6 kV
Cu-tape soldered to SD card, near side from HDMI connector	Yes	6 kV
Cu-tape soldered to SD card, far side from HDMI connector	Yes	No failure up to 10 kV
USB cable GND	No	6 kV
USB cable GND	Yes	No failure up to 10 kV

the copper patches. A 10 MΩ resistor was connected between the ground of the DUT and the large ground plane to discharge the charges accumulated in the DUT after each discharge. The experiments were done for two different cases: 1) with the SoC shield placed over the SoC region; and (2) without the shield. The ESD generator voltage was increased up to 10 kV and if a soft failure was observed, the threshold voltage was recorded. The failure signatures were system freeze, black screen, and white lines on the screen. Table I summarizes the results of the soft failure sensitivity of the DUT. The results show that when the SoC was not shielded, soft failures occurred by injecting

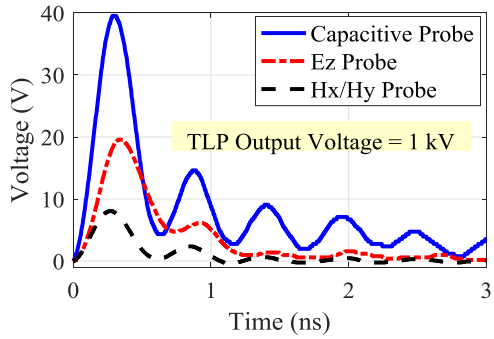


Fig. 4. TLP probe calibrations.

ESD at any connector. When the SoC was shielded, soft failures occurred when ESD was injected to the HDMI cable GND or to the near side of the SD card shell from the HDMI connector. Regarding these observations, two failure mechanisms with the same failure signature can be considered in this DUT. The first mechanism is direct field coupling from HCP to the CPU. The soft failure occurred because of this mechanism when the SoC region is not shielded. This failure mechanism is called "SoC field coupling" mechanism. The second failure mechanism is coupling to the HDMI components at both sides of the PCB or to the HDMI pins in the connector. This failure mechanism continued to exist even when the SoC shield was in place. This failure mechanism is called "HDMI coupling" mechanism. Coupling to the HDMI components at the front side of the PCB can be due to the voltage difference between the PCB GND and HCP. Coupling to the HDMI components at the back side of the PCB can be due to the voltage difference between the PCB GND and the mag frame of the DUT. This can happen if the PCB GND does not have a perfect electrical contact with the mag frame. Coupling to the HDMI pins can be due to the voltage difference between the PCB GND and HCP, or it can be due to the direct field coupling from the ESD generator tip to the HDMI pins. The coupling path which causes a soft failure in the HDMI coupling mechanism will be discussed later.

B. TLP Susceptibility Scanning (Step 2)

To investigate these failure mechanisms, TLP susceptibility scanning was performed on the DUT by using a TLP generator from Amber Precision Instruments Company [19]. The TLP output voltage is a pulse with 5 ns width and a 10–90% rise time of 400 ps. An 8 mm Ez probe and a 2 mm Hx/Hy probe were used to perform the TLP scanning. The calibration of these probes was obtained by injecting TLP via the probes on a 50-Ω transmission line and connecting the two ends of the line to two channels of the oscilloscope using two identical cables. The calibration results of these probes are presented in Fig. 4. Using Fig. 4, the coupled voltage for a known TLP output voltage can be obtained.

The susceptibility scanning was performed over the entire PCB at both sides, as well as on the connectors, and the occurrence of a soft failure was monitored. Table II summarizes the results of the susceptibility scanning on the DUT. It is observed from the TLP scan on the SoC region that the 25 MHz crystal

TABLE II
SUMMARY OF TLP SUSCEPTIBILITY SCANNING (STEP 2)

Injection position	Probe	TLP threshold voltage
SoC region		
25 MHz XTAL	Hx	0.2 kV
32 kHz XTAL	Hx	1 kV
Power Management IC	Hx	0.5 kV
PCB between memory ICs	Hx	0.5 kV
Left side of CPU package, above 25 MHz XTAL balls	Hx	0.4 kV
Left side of CPU package, above HDMI balls	Hx	0.5–2 kV
HDMI connector region		
HDMI connector area	Hx	5 kV
HDMI connector area	Ez	4 kV

TABLE III
SUMMARY OF TLP DIRECT INJECTIONS (STEP 3)

Injection position	Probe	TLP threshold voltage
SoC region		
Output pin of 25 MHz XTAL	Capacitive	6 V
Input pin of 25 MHz XTAL	Capacitive	25 V
HDMI connector region		
HDMI pins at connector	Capacitive	1–1.7 kV
HDMI CLK lines at back side of PCB	Capacitive	0.5 kV
HDMI CLK lines at series coupling capacitors	Capacitive	0.5 kV
Other HDMI lines at series coupling capacitors	Capacitive	1 kV

(XTAL) oscillator and the left side of the CPU package which is above the 25 MHz XTAL balls are the most susceptible parts in this region. The region around the HDMI connector was also found to be a susceptible region.

C. TLP Direct Injections (Step 3)

After susceptible regions of the DUT were identified, TLP direct injections on these regions were performed. At this step, the sensitivity of the signals and IC pins in the susceptible regions was quantified. If the soft failure sensitivity data of the ICs of the DUT had been available, there would have been no need to perform the TLP direct injections on the IC pins. The direct injections were performed by using a capacitive probe. The calibration of this probe is shown in Fig. 4 and the results of the TLP direct injections are summarized in Table III. It was observed that the output pin of the 25 MHz XTAL is the most sensitive pin in the DUT where the TLP output voltage of 6 V can cause a soft failure. By using the calibration result of the capacitive probe (see Fig. 4), it was found that injecting only 4.8 mA (i.e., $(6\,\mathrm{V} \times 40\,\mathrm{V})/(1000\,\mathrm{V} \times 50\,\Omega)$) for 500 ps at the output pin of the 25 MHz XTAL caused a soft failure. On the other hand, the HDMI clock (CLK) signals were found to be

TABLE IV
SUMMARY OF SYSTEM-LEVEL ESD TEST AFTER REMOVING HDMI SERIES COUPLING CAPACITORS

Zap position	SoC shield	Threshold voltage
HDMI cable GND shield	No	5 kV
HDMI cable GND shield	Yes	No failure up to 10 kV
Cu-tape soldered to SD card, near side from HDMI connector	Yes	No failure up to 10 kV

the most susceptible parts in the HDMI connector region. These signals are connected to the CPU via series coupling capacitors.

To check if disconnecting the path of the HDMI CLK signals to the CPU can prevent soft failure, another set of ESD experiments based on the HCP setup were performed by removing the HDMI series coupling capacitors connecting HDMI CLK lines to the CPU. The ESD was injected into the ground of the HDMI cable and SD card shell by using the Teseq ESD generator in contact discharge mode. The results of these measurements are summarized in Table IV. When the SoC region was not shielded, a soft failure occurred regardless of removing the HDMI series coupling capacitors. This is due to the fact that without the SoC shield, the soft failure occurs because of the direct field coupling from the HCP to the CPU (SoC field coupling mechanism). However, when the SoC region was shielded, no failures were observed when ESD was injected to the HDMI cable GND shield or to the SD card shell. These observations raised the following questions.

1) Which coupling path causes the soft failure in the HDMI coupling failure mechanism?
2) Why does the coupled ESD to the HDMI CLK lines cause the soft failure?

To answer the first question, four possible coupling paths in the HDMI coupling failure mechanism were investigated. The HDMI components and pins were shielded by copper tape to block coupling to the HDMI components and pins on both the front and back sides of the PCB. The coupling on the front side of the PCB and HDMI pins is due to the voltage difference between the PCB GND and HCP; coupling to the HDMI components on the back side of the PCB is due to the voltage difference between the PCB GND and the mag frame of the DUT. ESD was then injected by the ESD generator to the HDMI cable ground shield and SD card shell. It was observed that the soft failure occurred with the same ESD generator threshold voltage as before shielding these regions. Therefore, the only possible coupling path which remains is the field coupling from the ESD generator tip to the HDMI pins.

To investigate why the HDMI CLK signal connection is so sensitive even if HDMI is not used, the PCB layout of the DUT was reviewed. It was found that the HDMI CLK signals are routed next to the 25 MHz XTAL signals at layer 4 of the PCB (see Fig. 5). Since the output signal of the 25 MHz XTAL is the most susceptible signal in the DUT, the crosstalk of the ESD noise between the HDMI CLK and 25 MHz XTAL signals could be the reason for soft failure in the DUT when the SoC region is shielded. This coupled noise cannot be measured since there is

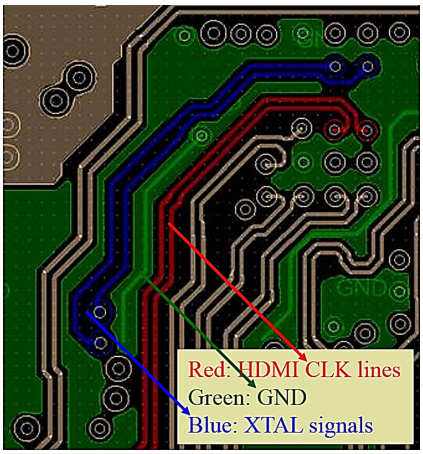


Fig. 5. HDMI CLK signals routed next to XTAL signals at layer 4 of the PCB of the DUT.

no access to the XTAL signals below the CPU. However, it can be investigated by performing full-wave simulation of the PCB of the DUT.

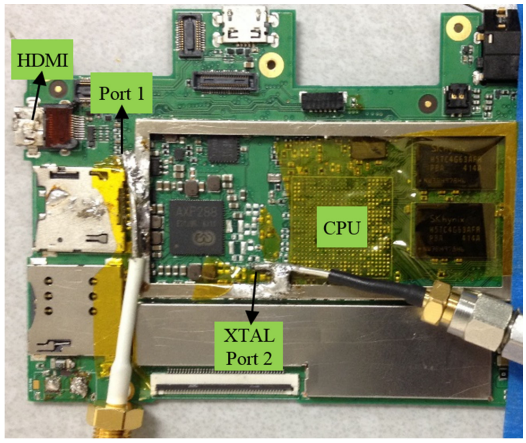
D. TLP Full-Wave Simulations (Steps 4–6)

The simulations were performed in CST Microwave Studio [20] by using the time-domain solver with finite integration technique. To reduce computational resources, the simulation model was simplified by considering only the region of the PCB which consists of the HDMI CLK and XTAL signals in the simulation. To increase the accuracy of the results, the metal thickness, as well as the dielectric and metal losses were considered (Step 4).

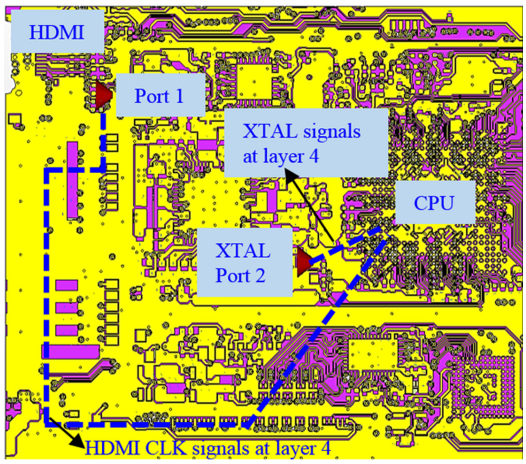
Before performing TLP simulation, the simulation model was validated by measurement. A two-port S-parameter measurement with the PCB of the DUT was performed and the results were compared with the simulation. The ports are considered at the HDMI CLK line next to the XTAL output signal and at the output pin of the XTAL. Fig. 6 shows the measurement and simulation setups. A good agreement was obtained between the simulation and measurement results as depicted in Fig. 7, which suggests that the simulation model can be further used for TLP simulations.

Since the CPU geometry cannot be imported in the CST simulation, it was modeled by terminating the HDMI CLK and XTAL signals at the CPU side by the corresponding CPU input impedances, which further simplified the simulation model. Since the CPU input impedance seen by the HDMI signals is 50 Ω, the HDMI CLK signals were terminated by 50 Ω resistors at the CPU side. The CPU input impedances seen by the output and input signals of the XTAL are provided by the CPU manufacturer. Based on the provided information, the output signal of the XTAL was terminated at the CPU side by a 1 MΩ resistor in parallel with a 1 pF capacitor, and a 5 kΩ resistor in parallel with a 1 pF capacitor was used to terminate the input signal of the XTAL at the CPU side (Step 4).

In the TLP simulation, the HDMI CLK line next to the output signal of the 25 MHz XTAL was excited with a current source defined at the HDMI series coupling capacitor position (Step 5).



(a)



(b)

Fig. 6. Two-port S-parameter: (a) measurement and (b) simulation setups.

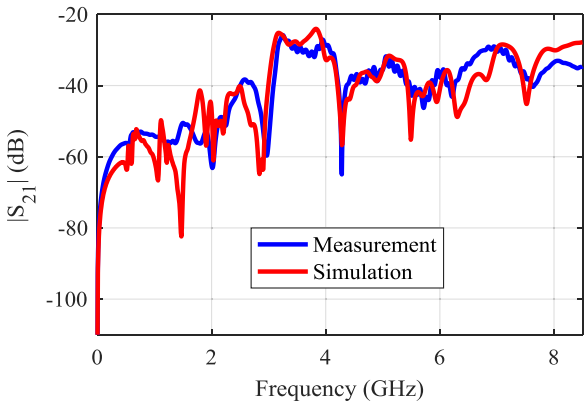


Fig. 7. Comparison of $|S_{21}|$ from measurement and simulation on the PCB of the DUT.

The excitation current is the same as the measured injected current with the capacitive probe to a 50 Ω transmission line when the output voltage of the TLP is 0.5 kV. This voltage (i.e., 0.5 kV) is the threshold voltage which causes the soft failure when the TLP pulse is injected with the capacitive probe to the HDMI CLK signals. Fig. 8 shows the excitation current used in the CST simulation. This waveform was obtained by

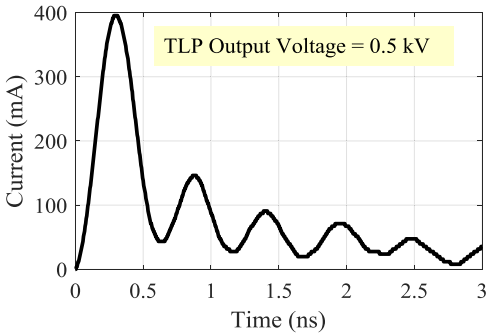


Fig. 8. Injected current with the capacitive probe at HDMI CLK signal (used in the TLP direct injection measurement (Step 3) and in the simulation).

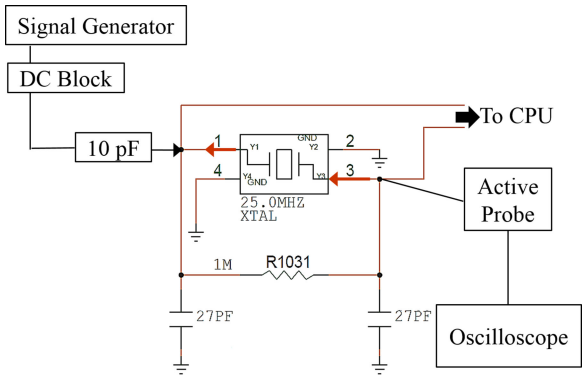


Fig. 9. Measurement setup to overwrite the clock of the XTAL.

dividing the capacitive probe calibration result shown in Fig. 4 by $2 \times 50\,\Omega$ (Step 5).

Simulation results show that the maximum coupled current from the HDMI CLK signal to the output signal of the 25 MHz XTAL at the CPU side is 6.4 mA for only 500 ps. Since it was noticed from the TLP measurements that injecting 4.8 mA TLP pulse for 500 ps into this signal causes the soft failure, it can be concluded that the TLP pulse coupling from HDMI CLK signals to the output signal of the 25 MHz XTAL is the cause of the soft failure in the DUT (Step 6). To prove this hypothesis, another measurement was done in the next section.

E. Robustness of the Clock Generation Circuit

If the coupling from HDMI CLK signals to the XTAL output signal causes the soft failure in the tablet, then by making the clock signal stronger, the system should become robust against the coupled TLP pulse to the XTAL signal. Consequently, the TLP threshold voltage which causes the soft failure should increase significantly. To make the clock of the system stronger, the XTAL clock was overwritten by an external clock from a signal generator. Before adding the external clock, the XTAL clock was probed. An active probe was used at the input pin of the XTAL to monitor the XTAL signal without disturbing the clock. Then, a 25 MHz signal from the signal generator was added to the output pin of the XTAL. A 10 pF capacitor was mounted at the XTAL output pin to ensure that the loading does not inhibit the external clock. Fig. 9 shows the measurement setup.

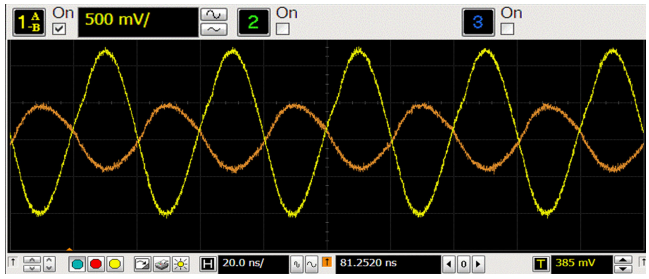


Fig. 10. Clock signal before (orange) and after (yellow) overwriting.

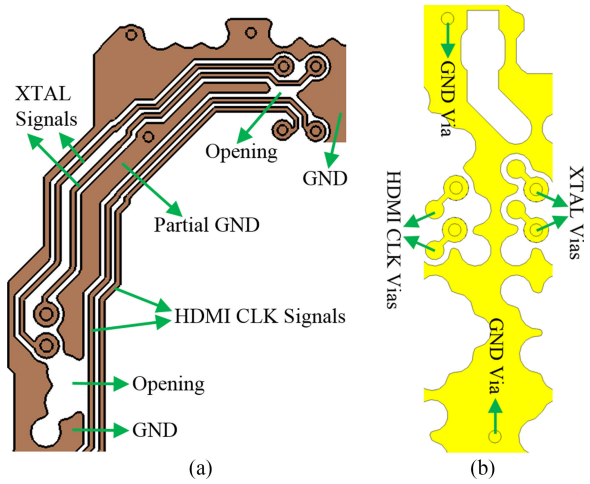


Fig. 11. HDMI CLK and XTAL signals routing in the original PCB design: (a) layer 4 and (b) top layer at CPU side.

The XTAL clock was overwritten by slowly increasing the amplitude of the external clock up to two times that of the XTAL signal (see Fig. 10). To investigate the robustness of the system after adding the external clock, TLP was injected with the capacitive probe to the HDMI CLK signals. When the signal generator output was turned off, the TLP threshold voltage was about 200 V. The decrease in the threshold voltage compared to Table III (i.e., 500 V) is due to the modification on the input and output pins of the XTAL. These modifications, which were related to monitoring the XTAL signal and the external clock injection, made the XTAL more sensitive to the TLP pulse. After adding the external clock, the soft failure occurred at 1.2 kV, which is six times higher than the threshold voltage when the DUT operates with XTAL clock. This indicates that after overwriting the XTAL clock, a stronger TLP pulse coupling from the HDMI CLK signals to the XTAL signals was needed to disturb the system.

F. Design of Countermeasures (Step 7)

In this section, the reason for the crosstalk between the HDMI CLK lines and XTAL signals is investigated first. Then, modifications in the PCB design are proposed to reduce this crosstalk.

By reviewing the PCB design file of the DUT, it is noticed that there is a partial ground between the HDMI CLK and XTAL signals [see Fig. 11(a)]. This ground is open at two sides which makes the coupling possible between the HDMI CLK and XTAL

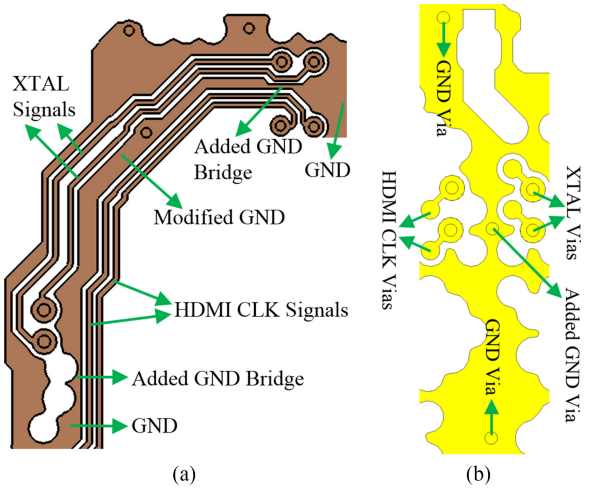


Fig. 12. Modified PCB layout to reduce the crosstalk (a) improvement in the ground between HDMI CLK and XTAL signals and (b) adding a ground via between HDMI CLK and XTAL vias at the CPU side.

TABLE V
SUMMARY OF SIMULATED TLP PULSE COUPLING BETWEEN HDMI CLK AND XTAL SIGNALS BEFORE AND AFTER PCB MODIFICATIONS

PCB design	Peak coupled current at the XTAL output signal
Original PCB design	6.4 mA
After closing GND between HDMI CLK and XTAL signals at layer 4	5.2 mA
After adding a GND via between HDMI CLK and XTAL_IN vias	2.3 mA
After adding a GND via between HDMI CLK and XTAL_IN vias and closing GND between HDMI CLK and XTAL signals	1.1 mA

lines. As the first modification of the PCB layout, the openings in the partial ground between these signals are closed as shown in Fig. 12(a). By simulating the TLP pulse injection on the modified PCB, a reduction of about 19% in the crosstalk was achieved.

The other source of coupling from the HDMI CLK signals to XTAL signals is due to the proximity of the vias of the corresponding signals. These signals are directly routed from layer 4 of the PCB to the top layer and there is no ground via between the vias of these signals, as shown in Fig. 11(b). Therefore, TLP pulse can be coupled from the HDMI CLK vias to XTAL vias. By adding one ground via between the HDMI CLK and XTAL vias [see Fig. 12(b)], the crosstalk between HDMI CLK and XTAL signals was reduced by 64%.

By considering these modifications, about an 83% reduction in the crosstalk between the HDMI CLK and XTAL signals was achieved. The coupled TLP noise current was about 1.1 mA after applying these modifications on the PCB layout. Based on the TLP measurement results, this amount of coupled TLP noise cannot disturb the system. Table V summarizes the improvement in the TLP noise coupling after performing the modifications.

It is worth mentioning that if the soft failure sensitivity of the CPU IC of the DUT was available, then the XTAL pin would have been identified as extremely sensitive in advance; i.e., before the reference design was released. Then, the occurrence of a possible soft failure could be predicted by utilizing full-wave TLP simulations of the PCB and comparing the coupled TLP pulse to the XTAL pin with the threshold value known from soft failure sensitivity data of the CPU. Therefore, the existing soft failure problem could be avoided with a proper design knowing the sensitivity of the XTAL output signal. For instance, the XTAL signals could be routed in a different layer and far away from the HDMI or any other I/O signals. In this way, ESD noise coupled from the connector to the data signal could not be coupled to the XTAL signals.

IV. CONCLUSION

A methodology was presented to analyze ESD-induced soft failures in electronic devices. Using this methodology, the root causes of the soft failures can be identified and countermeasures can be designed against the ESD-induced soft failures. In the proposed methodology, TLP full-wave simulations were performed after characterizing the soft failure behavior of the DUT ICs by performing some ESD and TLP measurements. The susceptible signals in the DUT can be identified by comparing the simulated voltages and/or currents at the DUT signals terminations with the threshold values obtained from the soft failure sensitivity process. If the simulated voltages and/or currents were higher than the threshold values, the signal was considered as susceptible and a soft failure could occur in the DUT. Using the simulation and measurement results allowed the root causes of the soft failures to be identified and the effect of countermeasures to be studied. As a case study, the root causes of the soft failures on a commercial tablet were determined by utilizing the proposed methodology. Since the soft failure sensitivity data of the ICs used in the DUT were not available, ESD susceptibility tests had to be performed on the DUT. By utilizing full-wave simulations and ESD and TLP measurements results, the root causes of the failures were identified. Then, countermeasures against the soft failures were designed with the aid of simulations and the DUT's susceptibility data obtained from measurements. It is worth mentioning that if the soft failure sensitivity data of the CPU IC of the DUT were obtained prior to finalizing the design of the product, then the soft failures could have been predicted by performing the proposed methodology. Subsequently, the design of the product could be improved to prevent the soft failures in the final product. As future work, the authors are working on developing a methodology in which the occurrence of the soft failures can be predicted via full-wave simulations without knowing the ESD susceptibility of the device. One of the main challenges will be the identification of soft failure due to coupled ESD noise to a very sensitive IC pin (like the DUT considered in this paper).

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